Pathway for ferroelectric memory with low voltage operation using ultra-thin $Hr_{0.5}Zr_{0.5}O_2$

K. Toprasertpong[1*], K. Ito[1], Z. Cai[1], K. Tahara[1], M. Takenaka[1], S. Takagi[1]

[1]*The University of Tokyo, 7-3-1 Hongo, Bunkyo, Tokyo 113-8656, Japan*

HfO_2-based ferroelectric thin films, particularly $Hf_{0.5}Zr_{0.5}O_2$ (HZO), have shown its potential for non-volatile memory with excellent CMOS compatibility, high density, and low power consumption. The commonly-employed ferroelectric thickness of 10 nm leads to an operating voltage of around 3-4 V, which is high as compared to current logic and DRAM technology. In this paper, we report our systematic work studying the operating voltage lowering by thickness down scaling of the ferroelectric layer. We demonstrated that the operating voltage of TiN/HZO/TiN capacitors can be lowered to 1.2 V or even below 1 V by scaling the HZO thickness down to 4 nm (Fig. 1) [1]. We also found that thinner HZO films not only achieve lower operating voltage, but also achieve higher endurance due to the improvement of the breakdown voltage. On the other hand, the wake-up effect becomes more pronounced in thinner films: our TiN/HZO (4 nm)/TiN capacitor initially has a pinched hysteresis loop and requires 10^6 cycles of electric field cycling to unpinch the hysteresis loop. We have gained an understanding of this wake-up behavior through modeling of oxygen migration inside the HZO film (Fig. 2) [2]. The pinched hysteresis loop is attributed to the domain pinning caused by the oxygen vacancies near the electrode interface. The oxygen vacancy distribution has been reported to be around 2 nm from each side of the electrodes, so its impact is expected to be severe for films around 4 nm or less. The wake-up occurs with the annihilation of oxygen vacancies with the oxygen migrating during electric field cycling, supported by its field dependence, temperature dependence, and model simulations. The wake-up frequency is optimal when it matches with the oxygen migration time inside the HZO film. We also applied thin HZO films to the gates of Si-channel ferroelectric FETs (FeFET) to realize FeFETs with low voltage operation [3]. The FeFET with 4 nm-thick HZO shows large memory window with almost wake-up-free characteristics, different from TiN/HZO/TiN capacitors. FeFETs with thin HZO show better endurance because of less interface degradation during polarization switching.

Acknowledgments

This work was supported in part by TSMC-JDP, JST CREST Grant Number JPMJCR20C3, and JSPS KAKENHI Grant Number 21H01359, Japan.

References

[1] K. Toprasertpong, K. Tahara, Y. Hikosaka, K. Nakamura, H. Saito, M. Takenaka, and S. Takagi, *ACS Appl. Mater. Interfaces*, vol.14, no. 45, pp. 51137-51148, Nov. 2022.

[2] K. Ito, M. Takenaka, S. Takagi, and K. Toprasertpong, 2025 Symposia on VLSI Technology and Circuits, T11-1, 2025

[3] Z. Cai, K. Toprasertpong, M. Takenaka, and S. Takagi, IEEE Transactions on Electron Devices 71(6), pp. 3633-3639, Jun. 2024.

* Corresponding author: toprasertpong@mosfet.t.u-tokyo.ac.jp

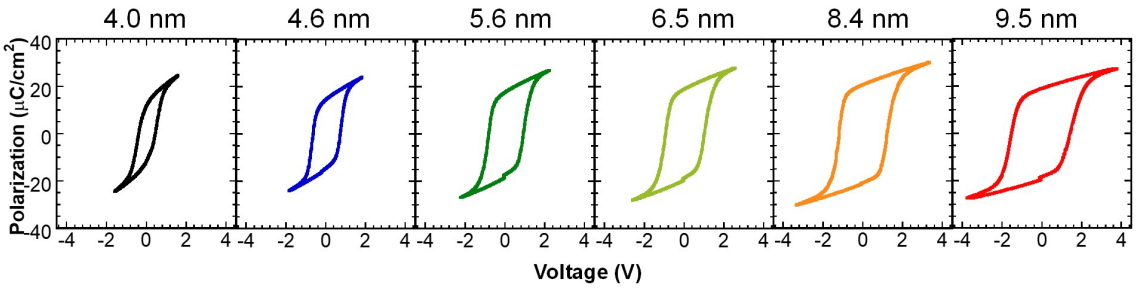

Fig. 1 *P-V* hysteresis loop of TiN/HZO/TiN capacitors with HZO thickness varied from 4 to 10 nm. Thickness down scaling of HZO results in lower polarization switching voltage.

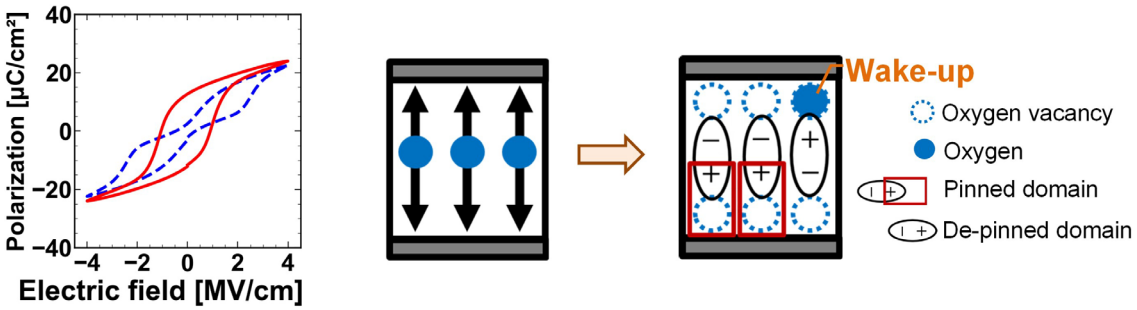

Fig. 2 Wake-up effect in ferroelectric capacitors with thin HZO and wake-up modeling. The wake-up effect is modelled by the oxygen vacancy annihilation with oxygen migrating in the HZO film.